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BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
MEW, KEVIN D	

ART UNIT	PAPER NUMBER
2664	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,907	ATARIUS ET AL.	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-24,27-32,35-42,44-47,49,50,52,56,59-61,63-65,67,68,70,71 and 73-76* is/are rejected.

7)☒ Claim(s) *10,11,25,26,33,34,43,48,51,53-55,57-58,62,66,69 and 72* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/4/2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,5,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

In particular, the abstract is objected to because it exceeds 150 words in length. Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

Reference numerals 10 and 20 in Fig. 3, reference numerals 10, 11, 12, 13, 14, 20, 21 in Fig. 5, reference numerals 100, 110, 120, 130, 140, 150, 160, 170, 180 in Fig. 6, reference numerals 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 in Fig. 7, reference characters 503a, 503b, 503c in Fig. 10, reference numeral 19 and reference characters 12-1 – 12-n in Fig. 11, reference characters 12-1 – 12-n in Figs. 12 and 13, reference characters 570a1-570a-n, and reference characters 503a, 503b, 503c, 501, 502, 504-1 – 504-2, 508 in Fig. 15A.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Reference characters 503b-1 – 503b-4, 503n-2 – 503n-4 in Fig. 10 and reference characters 508-1 in Fig. 15A.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1, 34 are objected to because of the following informalities:

In claim 1, the term "the" should be replaced with "a" as recited in "the local frequency reference" in line 4 of the claim. Appropriate correction is required.

In claim 34, the term "estimate" in line 3 of the claim should read "estimates." Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-9, 12-15, 16-24, 27-30, 73-76** are rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art, Easton (USP 5,764,687).

Regarding claims 1 & 16, Easton discloses a transceiver to perform a method for processing code division multiple access signals received (**analog transmitter and receiver for demodulating a signal in a spread spectrum multiple access communication system**, see lines 1-4, col. 2, lines 41-43, col. 8 and lines 23-26, col. 7, and element 16, Fig. 2) through at least one multipath propagation channel (**the searcher searches out windows of offsets likely to contain multipath signal peaks suitable for assignment of the fingers**, see elements 14, 12a-c, Fig. 1) to produce at least one relative frequency error estimate (**frequency error**, see element 44, Fig. 3), comprising:

a processor (**analog transmitter and receiver**, see element 16, Fig. 1) for receiving and processing the signals using the local frequency reference oscillator to obtain representative complex numerical samples (**I and Q channel samples**) for processing (**analog transmitter and receiver containing a downconverter chain that outputs digitized I and Q channel samples at baseband and the sampling clock used to digitized the received waveform is derived from a voltage controlled local oscillator**, see lines 11-15, col. 5 and elements 16, 40, Fig. 2);

channel estimators for correlating (**dispreading**) the complex numerical samples (**I and Q chip samples are provided to QPSK despreaders**, see elements 104a and 104b, Fig. 3) with shifts of a locally generated despreading code (**I and Q PN sequences are generated from PN sequence generator**, see Fig. 3) and producing a number of complex channel estimates (**output of on-time despreader**, see line 53, col. 9 and signals going into Pilot Filers, Fig. 3), each corresponding to a different delayed ray of the at least one multipath propagation channel (**I and Q PN sequences are generated from PN sequence generator, which are delayed from their counterpart sequences in the base station by the multipath propagation delay from the base station to the mobile unit**, see lines 24-38, col. 9 and element 106, Fig. 3);

frequency error estimators (**cross product circuits**, see element 146, Fig. 3; note that one cross product circuit is used for each finger) for computing a frequency error estimate (**frequency error**, see element 44, Fig. 3) for each ray based on successive values of a respective one of the channel estimates (**each finger makes an estimate of the frequency error using the cross product operator**, see lines 39-47, and equation 3, col. 6 and Fig. 3); and

at least one summer (**frequency error combiner**, see element 26, Fig. 2) for performing a weighted summation of the frequency error estimates to provide at least one relative frequency error estimate (**frequency error estimate from each finger 44a-c are combined and integrated in the frequency error combiner to generate an integrator output to adjust the clock frequency in order to compensate for the frequency error of the local oscillator**, see lines 48-54, col. 6 and Fig. 2).

Regarding claims 2 & 17, Easton discloses the transceiver of claim 1 to perform the method of claim 16, wherein the relative frequency error estimate is used to control the frequency of a local frequency reference oscillator (see lines 48-54, col. 6).

Regarding claims 3 & 18, Easton discloses the transceiver of claim 1 to perform the method of claim 16, wherein the frequency error estimator computes the frequency error estimate by multiplying the current value of the respective channel estimate with the complex conjugate of a previous value of the same channel estimate and using the product as the frequency error estimate for the respective ray (see lines 41-47, col. 6 and equation 3 and lines 13-16, col. 11).

Regarding claims 4 & 19, Easton discloses the transceiver of claim 2 to perform the method of claim 1, wherein the relative frequency error estimate is used to control the frequency of the local frequency reference oscillator in such a direction as to reduce the relative frequency error estimate (see lines 48-54, col. 6).

Regarding claims 5 & 20, Easton discloses the transceiver of claim 4 to perform the method of claim 1, further comprising an integrator for integrating the relative frequency error estimate to produce a control signal for controlling the frequency of the reference oscillator (see lines 48-53, col. 6).

Regarding claims 6 & 21, Easton discloses the transceiver of claim 2 to perform the method of claim 1, wherein the local frequency reference oscillator is used to control a transmit frequency (see lines 16-20, 22-25, col. 11).

Regarding claims 7 & 22, Easton discloses the transceiver of claim 1 to perform the method of claim 1, wherein the channel estimator correlations are made using the despreading code of a pilot signal (see lines 53-55, col. 9 and elements 114 and 116, Fig. 3).

Regarding claims 8 & 23, Easton discloses the transceiver of claim 2 to perform the method of claim 17, further comprising a rake combiner (see line 18, col. 8 and element 12, Fig. 3) for despreading a desired signal (see element 108, Fig. 3) using shifts of a locally generated wanted signal despreading code (Walsh sequence generated by the Walsh sequence generator, see element 100, Fig. 3) to produce one complex sample per data symbol per shift (see lines 46-50, col. 9) and for performing a weighted summation of the complex samples per shift using weighting factors (scaled by the strength of the pilot) based on the channel estimates to produce a rake-combined value (see element 42, Fig. 3) for each data symbol (see lines 27-32, col. 10 and element 130, Fig. 3).

Regarding claims 9 & 24, Easton discloses the transceiver of claim 8 to perform the method of claim 23, further comprising a decoder (see element 28, Fig. 2) for decoding the per-symbol rake-combined values using a soft error correction decoder to reproduce wanted information bits (see lines 7-19, col. 6).

Regarding claims 12 & 27, Easton discloses the transceiver of claim 8 to perform the method of claim 23, wherein the locally generated despreading code is a pilot code (pilot pair, see lines 53-55, col. 9 and elements 114 and 116, Fig. 3), and the locally generated data despreading code is a different code (Walsh sequence, see 41-50, col. 9).

Regarding claims 13 & 28, Easton discloses the transceiver of claim 8 to perform the method of claim 23, wherein the locally generated despreading code is a segment of the locally generated data despreading code during a period of time when the data symbols are equal to known pilot symbols (see lines 27-32, col. 10 and Fig. 3).

Regarding claims 14 & 29, Easton discloses the transceiver of claim 2 to perform the method of claim 17, wherein the signals used to control the frequency of the transceiver are received from one base station (see lines 13-24, col. 3, and Fig. 1).

Regarding claims 15 & 30, Easton discloses the transceiver of claim 2 to perform the method of claim 17, wherein the at least one summer produces at least one relative frequency error estimate separately for each base station (see lines 59-65, col. 4 and element 26, Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 31-32, 35-42, 44-47, 49-50, 52, 56, 59-61, 63-65, 67-68, 70-71** are rejected under 35 U.S.C. 103(a) as being unpatentable over Easton in view of Shohara (US Publication 2003/0087617).

Regarding claims 31 & 41, Easton discloses a transceiver to perform the method for processing code division multiple access signals received through at least one inultipath propagation channel to produce at least one relative frequency error estimate, comprising:

a processor (**analog transmitter and receiver**, see element 16, Fig. 1) for receiving and processing the signals using the local frequency reference oscillator to obtain representative complex numerical samples (**I and Q channel samples**) for processing (**analog transmitter and receiver containing a downconverter chain that outputs digitized I and Q channel samples at baseband and the sampling clock used to digitized the received waveform is derived from a voltage controlled local oscillator**, see lines 11-15, col. 5 and elements 16, 40, Fig. 2);

despreaders (**despreaders**, see element 104, Fig. 3) for different delayed rays of the multipath channel for correlating the numerical samples (**despreaders are provided with I and Q chip samples**) with different shifts of a locally generated wanted signal

despreading code (**despreaders also receive I Q PN sequence generated by the PN sequence generator are delayed from their counterpart sequences in the base station by the multipath propagation delay from the base station to the mobile unit**, see lines 26-35, col. 9) over symbol intervals to produce streams of complex despread values corresponding to each ray and successive symbol interval (**output of depreaders produces a pilot pair for PI(n) and PQ(n) symbol n**, see lines 33-35, col. 9)

channel estimators for processing (**dispreading**) the frequency-corrected despread value streams (**I and Q chip samples are provided to QPSK despreaders with I and Q PN sequences are generated from PN sequence generator**, see elements 104a and 104b, Fig. 3) to produce complex channel estimates for each ray (**output of on-time despreader is pair of pilot I and pilot Q**, see line 53, col. 9 and signals going into Pilot Filers, Fig. 3);

frequency error estimators (**cross product circuits**, see element 146, Fig. 3; note that one cross product circuit is used for each finger) for determining a frequency error estimate (**frequency error**, see element 44, Fig. 3) for each ray based on successive values of a respective one of the channel estimates (**each finger makes an estimate of the frequency error using the cross product operator**, see lines 39-47, and equation 3, col. 6 and Fig. 3); and

at least one combiner (**frequency error combiner**, see element 26, Fig. 2) for combining the frequency error estimates to provide at least one relative frequency error estimate (**frequency error estimate from each finger 44a-c are combined and integrated in the frequency error combiner to generate an integrator output to**

adjust the clock frequency in order to compensate for the frequency error of the local oscillator, see lines 48-54, col. 6 and Fig. 2).

Easton also discloses that the rotation rate of the pilot vector in the I and Q space would be measured (see lines 39-44, col. 6), which teaches that the pilot I and Q samples would be phase rotated before being measured. Easton does not explicitly disclose frequency error correctors for correcting frequency errors on each of the despread value streams by progressively rotating the phase angle of successive despread values at a rate given by an associated frequency error integral.

However, Shohara discloses a DL phase rotator (see element 20, Fig. 1) in a radio communications system (see lines 9-12, paragraph 0031) in which successive I and Q sample pairs are digitally rotated with sample-to-sample phase rotation rate that is determined by the downlink frequency offset command (see lines 29-38, paragraph 0033).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to combine the CDMA transceiver and method of Easton with the DL phase rotator of Shohara such that the DL phase rotator would correct the frequency error before passing the complex I and Q samples to the frequency error estimator, such as the DL phase rotator taught by Shohara. The motivation to do so is for the DL phase rotator to act as a digital frequency shifter for the complex baseband received samples with the purpose of removing receiver frequency error because the frequency error of the samples must be small enough to ensure accurate data demodulation.

Regarding claims 32 & 42, Easton discloses the transceiver of claim 31 to perform the method of claim 41, wherein the at least one relative frequency error estimate is used to control the frequency of a local frequency reference (see lines 48-54, col. 6).

Regarding claims 35 & 45, Easton discloses the transceiver of claim 32 to perform the method of claim 42, wherein the local frequency reference oscillator is used to control a transmit frequency (see lines 16-20, 22-25, col. 11).

Regarding claims 36 & 46, Easton discloses the transceiver of claim 32 to perform the method of claim 42, further comprising a rake combiner (see line 18, col. 8 and element 12, Fig. 3) for despreading a desired signal (see element 108, Fig. 3) using shifts of a locally generated wanted signal despreading code (Walsh sequence generated by the Walsh sequence generator, see element 100, Fig. 3) to produce one complex sample per data symbol per shift (see lines 46-50, col. 9) and for performing a weighted summation of the complex samples per shift using weighting factors (scaled by the strength of the pilot) based on the channel estimates to produce a rake-combined value (see element 42, Fig. 3) for each data symbol (see lines 27-32, col. 10 and element 130, Fig. 3).

Regarding claims 37 & 47, Easton discloses the transceiver of claim 36 to perform the method of claim 46, further comprising a decoder (see element 28, Fig. 3) for decoding the per-symbol rake-combined values using a soft error correction decoder to reproduce wanted information bits (see lines 7-19, col. 6).

Regarding claims 39 & 49, Easton discloses the transceiver of claim 31 to perform the method of claim 41, wherein the signals are received from one base station (see lines 13-24, col. 3, and Fig. 1).

Regarding claims 40 & 50, Easton discloses the transceiver of claim 31 to perform the method of claim 41, wherein the combiners produce frequency error estimates separately for each base station (see lines 59-65, col. 4 and element 26, Fig. 2).

Regarding claim 44, Easton discloses the method of claim 42, wherein the step of combining includes adding the frequency error estimates and obtaining a relative frequency error estimate and integrating the relative frequency error estimate using an outer loop integrator to produce the control signal (see lines 48-54, col. 6).

Regarding claim 52, Easton discloses the transceiver of claim 36, further comprising an error correction and detection decoder for soft-decoding a block of the rake-combined values to provide an error indication for successively recurring block intervals (see lines 7-19, col. 6).

Regarding claim 56, Easton discloses the method of claim 46, further comprising soft-decoding a block of the rake combined values to provide an error indication for successively recurring block intervals (see lines 7-19, col. 6).

Regarding claim 59, Easton discloses the transceiver of claim 2, further comprising an outer loop integrator for integrating the frequency estimates to produce a control signal to control the local frequency reference oscillator to a value based on the received signal (see lines 48-54, col. 6).

Regarding claim 60, Easton discloses the transceiver of claim 1, further comprising a rake-combiner for combining and decoding the despread values to decode unknown data symbols.

Regarding claim 61, Easton discloses the transceiver of claim 60, wherein the rake-combiner comprises an error correction and error detection decoder to produce an error indication for the decoded symbols.

Regarding claim 63, Easton discloses the method of claim 17, further comprising:

integrating the relative frequency error estimate using an outer loop integrator to produce a control signal (see lines 48-50, col. 6); and

controlling the frequency of the local frequency reference oscillator using the control signal (see lines 50-54, col. 6).

Regarding claim 64, Easton discloses the method of claim 16, further comprising the step of rake-combining and decoding the despread values to decode unknown data symbols (see lines 7-19, col. 6).

Regarding claim 65, Easton discloses the method of claim 64, wherein the decoding comprises error correction and error detection decoding to produce an error indication for the decoded symbols (see lines 13-17, col. 6).

Regarding claim 67, Easton discloses the transceiver of claim 36, further comprising a rake-combiner for rake combining and decoding the despread values to decode unknown data symbols (see lines 7-19, col. 6).

Regarding claim 68, Easton discloses the transceiver of claim 67, wherein the rake-combiner comprises error correction and error detection decoder to produce an associated error indication for the decoded symbols (see lines 13-17, col. 6).

Regarding claim 70, Easton discloses the method of claim 41, further comprising rake-combining and decoding the despread values to decode unknown data symbols (see lines 13-17, col. 6).

Regarding claim 71, Easton discloses the method of claim 70, wherein the decoding comprises error correction and error detection decoding to produce an associated error indication for the decoded symbols (see lines 13-17, col. 6).

Regarding claims 73 & 75, Easton discloses an apparatus to perform the method for estimating a frequency error (**each finger makes an estimate of the frequency error**) between a local frequency reference of a receiver and carrier frequencies of one or

more transmitters (**to adjust clock frequency of local oscillator in the analog transmitter and receiver**, see lines 52-54, col. 6) comprising:

frequency error estimators for estimating frequency errors separately for each transmitter (**cross product circuits**, see element 146, Fig. 3; note that one cross product circuit is used for each finger); and

a combiner for combining the frequency error estimates to produce at least one relative frequency error estimate (**frequency error estimate from each finger 44a-c are combined and integrated in the frequency error combiner to generate an integrator output to adjust the clock frequency in order to compensate for the frequency error of the local oscillator**, see lines 48-54, col. 6 and Fig. 2).

Regarding claims 74 & 76, Easton discloses the apparatus of claim 73 to perform the method of claim 75, further comprising integrating the combined frequency error estimates (see lines 48-49, col. 6).

Allowable Subject Matter

7. Claims 10-11, 25-26, 33-34, 43, 48, 51, 53-54, 55, 57-58, 62, 66, 69, 72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter.

In claim 10, the transceiver of claim 9, further comprising an error detection decoder for performing an error check on the decoded information bits, and to generate an error or no-error indication, wherein the relative frequency error estimate is only used to control the local reference oscillator when a no-error indication is generated.

In claim 25, the method of claim 24, further comprising performing an error check on the decoded information bits and to generate an error or no-error indication, wherein the relative frequency error estimate is only used to control the local reference oscillator when a no-error indication is generated.

In claim 33, the transceiver of claim 32, further comprising inner loop integrators for integrating respective frequency error estimates to produce integrated frequency errors.

In claim 38, the transceiver of claim 37, further comprising an error detection decoder for performing an error check on the decoded information bits and to generate an error or no-error indication, wherein the relative frequency error estimate is only used to control the local reference oscillator when the no-error indication is generated.

In claim 43, the method of claim 42, further comprising integrating respective frequency error estimates using inner loop integrators to produce integrated frequency errors.

In claim 48, the method of claim 47, further comprising performing an error check on the decoded information bits and to generate an error or no-error indication, wherein the relative frequency estimate is only used to control the local reference oscillator when the no-error indication is generated.

In claim 51, the transceiver of claim 32, further comprising:

an inner loop integrator for integrating the frequency error estimate to produce inner loop integral values; and

an outer loop integrator for integrating the inner loop integral values to produce a control signal to control the local frequency reference oscillator to a value based on the received signal.

In claim 53, the transceiver of claim 52, wherein the outer loop integrator integrates the inner loop integral values only for blocks for which the error indication is indicative of no errors, and the inner loop integrator integrates the frequency error estimate only for blocks for which the error indication is indicative of no errors.

In claim 54, the transceiver of claim 52, wherein the combiner processes frequency error estimates corresponding to blocks of symbols that have been error correction and detection decoded and which have an associated error indication indicative of no errors.

In claim 55, the method of claim 42, further comprising:

integrating the frequency error estimates using an inner loop integrator to produce inner loop integral values; and

integrating the inner loop integral values using an outer loop integrator to produce a control signal to control the local frequency reference oscillator to a value based on the received signal.

In claim 57, the method of claim 56, wherein the step of integrating comprises integrating inner loop integral values only for blocks for which the error indication is indicative of no errors, and the step of integrating using an inner loop integrator

integrates the frequency error estimates only for blocks for which the error indication is indicative of no errors.

In claim 58, the method of claim 56, wherein the step of combining processes frequency error estimates corresponding to blocks of symbols that have been error correction and detection decoded and which have an associated error indication indicative of no errors.

In claim 62, the transceiver of claim 59, wherein the combiner adds the real parts of the per ray frequency error estimates to obtain a real sum and adding the imaginary parts to produce an imaginary sum and computing the two-argument arctangent of the real and imaginary sum.

In claim 66, the method of claim 63, wherein the combining step includes adding the real parts of the per-ray frequency error estimates to obtain a real sum and adding the imaginary parts to produce an imaginary sum and computing the two-argument arctangent of the real and imaginary sum.

In claim 69, the transceiver of claim 31, wherein the combiner adds the real parts of the per-ray frequency error estimates to obtain a real sum and adding the imaginary parts to produce an imaginary sum and computing the two-argument arctangent of the real and imaginary sum.

In claim 72, the method of claim 41, wherein the combining step includes adding the real parts of the per-ray frequency error estimates to obtain a real sum and adding the imaginary parts to produce an imaginary sum and computing the two-argument arctangent of the real and imaginary sum.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with respect to method and apparatus for automatic frequency control in a CDMA receiver.

US Patent 6,625,197 to Lundby et al.

US Patent 5,361,276 to Subramanian

US Patent 5,767,738 to Brown et al.

US Patent 6,304,620 to Rouphael

US Patent 6,137,843 to Chennakeshu et al.

Us Patent 5,490,165 to Blakeney, II et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 703-305-5300. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KDM
Art Unit 2664

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600